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Possible SCD/RSE Trigger Module

Real-Time Systems Engineering Department
Kurt Biery, Alan Prosser
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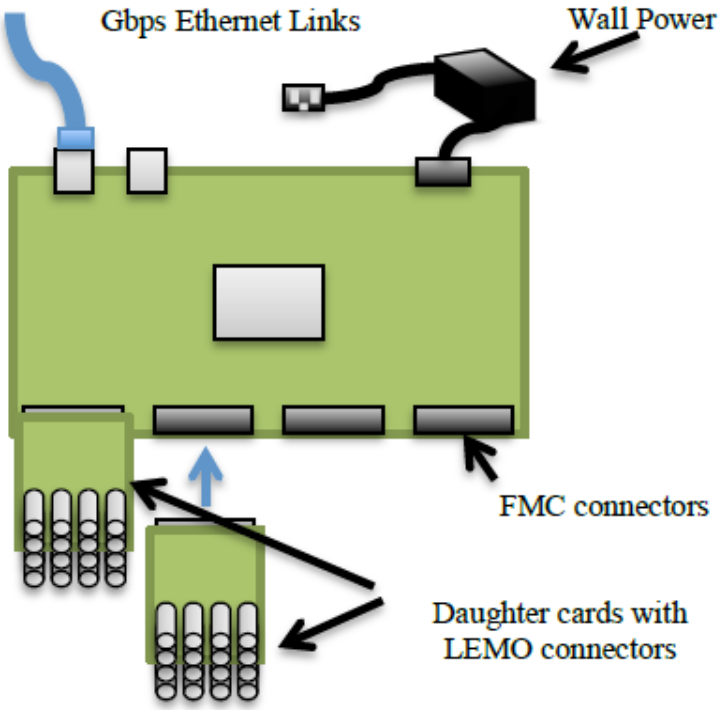
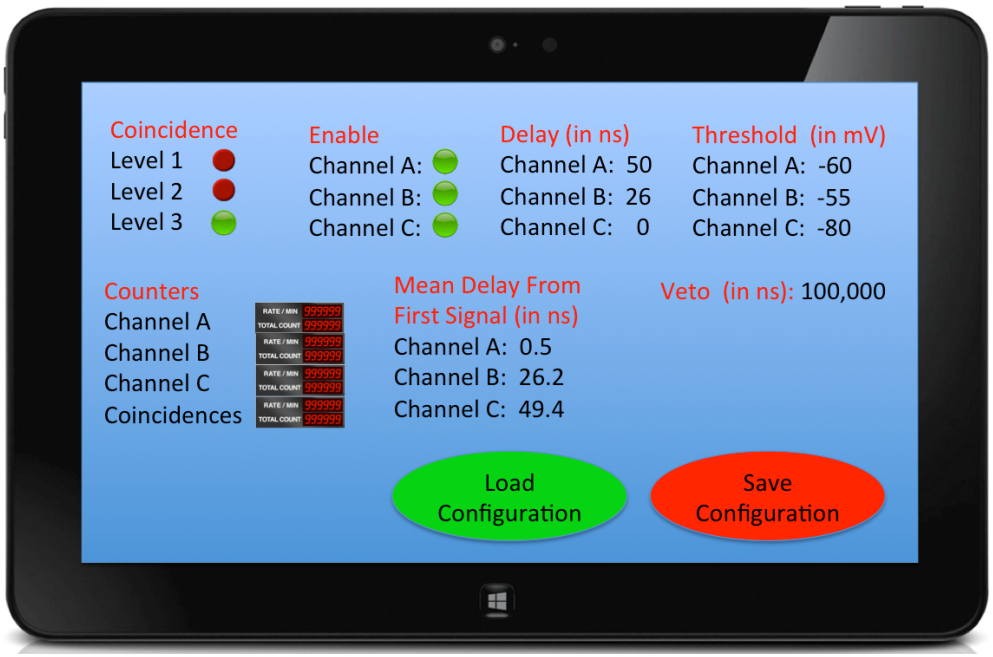
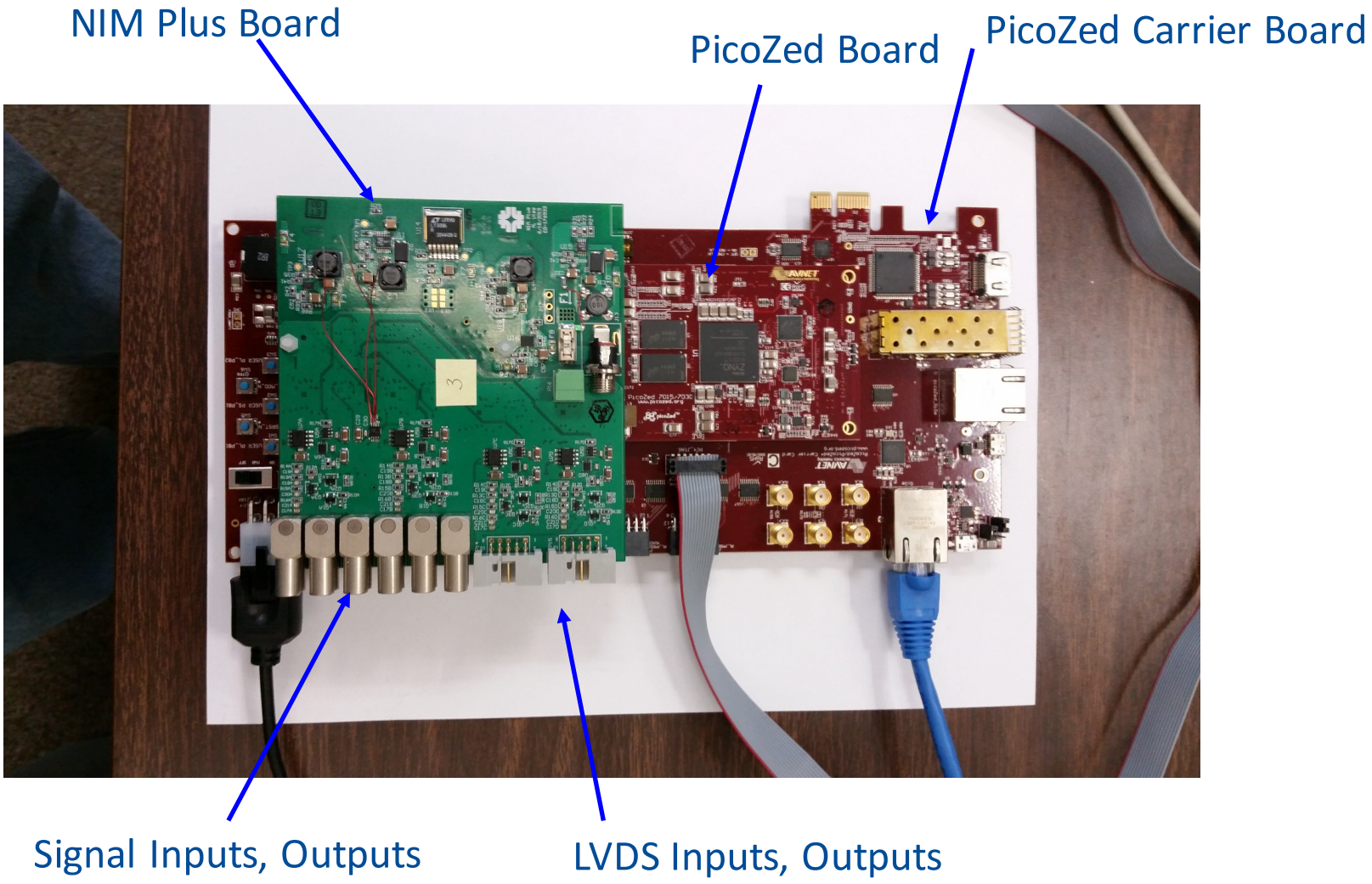
PREP in the FPGA Era

Vision: gradually replace aging commercial electronics with general-purpose FPGA boards and appropriate daughter cards

Initial candidate: NIM coincidence module






NIM Plus Board
PicoZed Board
PicoZed Carrier Board
Signal Inputs, Outputs
LVDS Inputs, Outputs

NIM Plus Board

- Input Channels (to FPGA):
  - 4 Analog Input Channels (LEMO Connector)
    - Each channel includes:
      - -2V to +3V Input Range with Buffer Op Amp
      - 12 bit DAC for threshold
      - LVDS Comparator Output (DAC vs Op Amp output) to FPGA via FMC
  - 4 LVDS Digital Logic Inputs (via 10 pin header)
- Output Channels (from FPGA):
  - 4 NIM Level Outputs (LEMO Connector)
  - 4 TTL/LVTTL Level Outputs (LEMO Connector)
  - 4 LVDS Outputs (via 10 pin header)

FPGA-Based NIM Coincidence Module

Hardware & Firmware

- Receive NIM or TTL or LVDS signals
- Look for coincidence of programmable number of signals
- Output signal can be delayed and/or stretched
- Internal clock provided, external may be possible
- BUSY signal

External Interface

- Web-based control and feedback

FPGA-Based NIM Trigger Module

Hardware & Firmware

- Receive NIM or TTL or LVDS signals
- Look for coincidence of programmable number of signals
- Output signal can be delayed and/or stretched
- Internal clock provided, external may be possible
- BUSY signal
- Accept INHIBIT signal to prevent generation of output signal
- Counters of input pulses, inhibit-ed output pulses, etc, etc

External Interface

- Web-based control and feedback
- Programmatic control and readout
- Readout of counters and composition of individual trigger decisions

Target Dates for Coincidence & Trigger Module Features

April 30th – development of the firmware, deployment on the PicoZed on the testbench, manual testing of all functions

June 30th – development of the web interface with control functionality, some amount of register readout, and some amount of counter readout

Later in the summer and fall:

- Programmatic interface
- Additional readout functionality (e.g. individual trigger composition)
- Diagnostic firmware and software
- Firmware and software for automated testing
- Documentation: user guide, tester guide, etc.

Longer-term – incorporation of this module into the PREP pool

Our Understanding of the SBND Trigger Module

1. Accept some number of NIM or TTL inputs and support configurable combinations of these inputs to generate an overall trigger signal
2. Support an "inhibit" signal that suppresses the output of the overall trigger signal
3. Keep internal counters on the number of each type of input triggers that were received within a given time interval, ditto the number of output trigger signals, ditto the number of times an input signal was inhibited. Probably also the wall-clock time spent inhibited. Provide a way to periodically read out these values.
4. Support event-by-event read out of which trigger signals went into the overall trigger
5. Rate needs?
6. Double-pulse separation needed?
7. Other requirements?

Questions and Suggestions from a meeting on 24-March

1. How will calibration of input signal thresholds be handled? (to be determined)
2. Are the trigger decisions pipelined? (This has now been added to the design.)
3. Stretch and/or delay input signals.
4. Prescale inputs.
5. Packaging is important: mechanical stability of connections; routing of cables in a real experiment.
6. Keep internal log of timestamps when signals are above threshold and the output is ON (for later readout and validation).
7. Multiple different output signals (trigger table).
8. Other options include the LArIAT CAEN module with firmware from Mike K. Also, the DarkSide-50 CAEN V1495 with FW from Boris B.
9. Talk more with Angela, Wes, Eric, and Georgia.

Backup Slides

Coincidence/Trigger Module Firmware Capabilities

- Complete “sum of products” terms for input selection
- Minimum detectable signal width: 1 ns
- Output pulse delay in increments of 1 ns**
- Output pulse width adjustable in increments of 4 ns
- No dead time for pulses that do not arrive in violation of output width interval

- *Assumes FPGA fabric clock period of T = 4ns (F = 250 MHz).
- ** Configured in firmware at compile time. Change requires update to firmware.
- ***Adjustable in software through user interface.